REMARKS

The application has been reviewed in light of the Office Action dated September 8, 2005. Claims 1-12 were pending. By this Amendment, new dependent claims 13-15 have been added. Accordingly, claims 1-15 are now pending, with claims 1 and 7 being in independent form.

The title was objected to as purportedly not sufficiently descriptive.

By this Amendment, the title has been amended to be more descriptive of the application.

Claims 1-12 were rejected under 35 U.S.C. §102(e) as purportedly anticipated by U.S. Patent No. 6,618,847 to Hulse et al.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1 and 7 are patentable over the cited art, for at least the following reasons.

This application relates to a layout design method for a multi-layered semiconductor integrated circuit. Applicant devised improved layout design techniques for a multi-layered semiconductor integrated circuit having multilevel metallization whereby power supply wiring does not need to be completely performed on the layout before wiring of signal lines is performed, and connection of the power supply wiring of an upper-layer metal and power supply wiring of a lower layer metal can be performed after the wiring of signal lines.

For example, independent claim 1 is directed to a layout design method for a semiconductor integrated circuit which includes providing a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells. Each filler cell acts to fill space between the functional cells. Moreover, one of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal. Another of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail, one of which is connected to the upper-

layer metal through a via. The cells are arranaged on a layout as follows: (a) the functional cells are arranged on the layout based on the structural information from the layout library; and (b) the filler cells of any of the plurality of groups are arranged selectively based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from signal lines on the layout. Thus, the connection of the power supply wiring of the upper-layer metal and the power supply wiring of the lower-layer metal is made through arrangement of the filler cells after the wiring of signal lines.

Hulse, as understood by Applicant, is directed to a layout design tool which allows a user to automatically intersperse capacitor filler cells around standard cell logic (see Hulse, lines 58-65). Hulse discloses at column 5, lines 25-43 that additional tools may be used in addition to the layout design tool to route wiring, based on a a generated netlist, to each of the components, and that metal layers, wiring layers, vias, connection pads are formed based on the routing information. Hulse further discloses at column 4, lines 58-65 that each of the capacitor filler cells includes power and ground rails.

However, Hulse does not disclose or suggest performing connection of power supply wiring of an upper-layer metal and power supply wiring of a lower layer metal in a multi-layered semiconductor integrated circuit having multilevel metallization, after the wiring of signal lines, as provided by the claimed invention of the present application.

Hulse merely states that the capacitor filler cells extend the power and ground rails from adjacent standard cells, but does not disclose or suggest that the filler cells are arranged to connect power supply wiring of an upper-layer metal and power supply wiring of a lower layer metal.

Applicant does not find disclosure or suggestion in the cited art, however, of a layout design method for a semiconductor integrated circuit which includes providing a cell layout

library which stores structure information of functional cells and a plurality of groups of filler cells, wherein one of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail, one of which is connected to the upper-layer metal through a via, as provided by the claimed invention of claim 1.

Independent claim 7 is patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1 and 7, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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